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AUTOMATIC ERROR-DETECTION SYSTEM FOR TOLL-GRADE TELEPHONE CIRCUIT DATA TRANSMISSION

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27 NOV 1961

ABSTRACT

A machine has been designed for automatic error detection in digital data transmissions over toll-grade telephone circuits. Because of the coding techniques used, the data link error rate is primarily a function of terminal equipment reliability and several other factors, including the synchronization between transmitter and receiver. This paper describes the general system, the logical design considerations, the hazards encountered, and the debugging and test methods used. Results indicate that the implementation has been successful.

Introduction

The use of telephone circuits for the transmission of digital data has increased rapidly in recent years. A number of modulation systems are available for signaling at rates from 800 to 2400 bits per second with measured long-term error rates of approximately one bit in 10^5 bits.[1] It is most significant that these errors are highly correlated. Measurements have shown that almost any well-designed modulation system will transmit essentially error-free bit sequences much in excess of 10^5 bits. These error-free periods are terminated by relatively short periods with many errors. As a result of the burst-like nature of the errors, investigations were made into optimum techniques for correcting these errors while still maintaining a low coding "overhead." The work of Fontaine and Gallager[2] has shown that the use of a (255, 231) Bose-Chaudhuri code[3] for error detection indicates, from an extrapolation of a 709 computer simulation using 2000 hours of toll-grade telephone line error patterns, the code would fail to detect erroneous words on the average of only once in 300 years. The mean time to failure of the code when faced with continuous high-level random noise is 38 days. A simple method for implementing these codes was subsequently developed by W. W. Peterson.[4] The use of these error-detection techniques to provide error-free data transmission by use of feedback communications techniques followed.[5]

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1. E. J. Hofmann, "Measured Error Distributions on the Bell A-1 Facility over Various Media," Proceedings of the National Electronics Conference, 1960, pp. 37-44.

2. A. B. Fontaine, R. G. Gallager, "Error Statistics and Coding for Binary Transmission over Telephone Circuits," Proc. IRE, Vol. 49, June 1961, pp. 1059-1064.

3. R. C. Bose, D. K. Ray-Chaudhuri, "On a Class of Error Correcting Binary Group Codes," Information and Control, pp. 68-79, March 1960.

4. W. W. Peterson, "Error-Correcting Codes," MIT Press and John Wiley and Sons, Inc., New York, N. Y., pp. 162-183, 1961.

5. B. Reiffen, W. Schmidt, H. Yudkin, "The Design of an 'Error-Free' Data Transmission System for Telephone Circuits," AIEE Winter General Meeting, January 1961.

Realizing the wide gap between the computer simulation and the successful implementation of these results in an "on-line" system, work was initiated on the design, construction, and testing of an "on-line" machine, BC-1, which embodied the Bose-Chaudhuri codes for error detection only.

General System Considerations

It would be well to describe the general (255,231) Bose-Chaudhuri error-detection method at the outset of system discussions. The particular notation indicates that the total sequence of bits is 255, of which 231 are data to be conveyed. The remaining 24 are parity-check bits. The encoding and decoding procedures are explained in Figure 1.

Because of practical limitations imposed by one of the modulation systems* with which the BC-1 operates and, since this error-detection method was planned to be the first step in an error-correction system which makes use of retransmission requests, the word format used for the machine is identical to that cited in reference 5 and is shown in Figure 2. The complete transmitted word consists of 256 bits. One bit is not encoded; it is part of the five bits of "space" bounding the paralleled SYNC signal for protection.+ The first five bits of the word are called filler bits. The next 224 are data bits; they contain the actual data being transmitted in the word. The next three are service bits which would ordinarily convey retransmission requests and information about the state of the channel in the final feedback system. The last 24 bits are the check bits of the (255, 231) Bose-Chaudhuri code.

The complete system diagram of the BC-1 is shown in Figure 3. At the transmitter a data generator delivers a predetermined

*. The BC-1 machine will operate with any data Modem having three parallel input and output signals. These signals are called TIMING, SYNC, and DATA; the first functions to convey bit-by-bit sampling time to the receiver, the second indicates the start of a word, and the third parallel line carries the true data. These signals are dipulses and form the standard interface signals between encoder and modulator and between demodulator and decoder.

+. The Bell A-1 Digital Data System, which uses these signals and is one of the modems with which the BC-1 can operate, must not have "mark" bits within two time slots of the SYNC position. Thus, the first five time slots in the 256-bit word contain no data.

pattern of 224 bits to the ENCODER unit. In this unit the word composition logic acts in a fashion similar to the switch in the upper part of Figure 1. This same logic also insures that the word format is identical to that indicated in Figure 2. The output of the ENCODER section is then connected to any suitable data modulation system and, thereafter, to any circuit desired. The output of the demodulator is then passed to the DECODER section where the word decomposition logic strips out the portions of words which are of interest to various logical subroutines. After passing through several criteria for determination of the validity of the message, the ERROR signal is, if necessary, emitted as a "D" (i.e., Detected error) signal.

In order to check on the effectiveness of the error-detection system implementation, the results of this technique are correlated with those based upon a bit-by-bit comparison of the data bits of the message. This is accomplished by having the word decomposition logic of the DECODER compare the 224 data bits with the output of the data generator which is aligned to give the same pattern of bits as the transmitting data generator and is synchronized to the incoming data. If a discrepancy occurs in the bit-by-bit comparison, then the comparison error logic will provide a "C" signal (i.e., Comparison error) which indicates that at least one bit of the data portion of the message is in error. The correlation of the errors detected by both methods is obtained by the C-D matching logic and three counters which maintain a record of the number of times each of the three combinations of interest occurs. Subsequent portions of this paper will deal with these sections in much greater detail and indicate some of the hazards and their solutions as determined in the logical design and operation of the BC-1.

Before proceeding into the design of the machine, it would be well to realize that the "300-year" figure mentioned for the effectiveness of the code merely indicates that the burden of reliability of the data transmitted is now placed at the terminal equipment rather than on the communications circuit. Long circuit outages are the exception here. Hence, it is the function of this machine to validate the computer simulation and to generate an awareness of those practical phenomena

that were not simulated on a computer because the hazards had not been or could not be foreseen. As a result of the experience gained from the design and test of the BC-1, the prototype of the complete feedback system, BC-2, will be a much more reliable device with the emphasis placed on the elimination of those hazards introduced by the feedback logic, rather than by both the feedback logic and error-detection system.

The Feedback Shift Register

One of the outstanding advantages of the Bose-Chaudhuri codes is the comparative ease with which they can be implemented. Using the techniques developed by W. W. Peterson[6], the particular code in which we are interested may be encoded and decoded by the linear feedback shift register shown in Figure 4.

During the encoding operation the parity bits are derived by driving each of the 231 bits of the "coded-over" portion of the message into the shift register. The feedback switch, which has been closed during this time, is then opened and the contents of the register are appended to the message as previously indicated.

The decoding is performed in a similar manner but it should be recognized that when the last (231st) bit of the message proper has entered the decoding shift register (the feedback switch has been closed during this time), the contents of the 24 stages of the decoding register should be identical to those of the encoding register. With the feedback switches in both units now open, the input to the decoding register is essentially a comparison between the contents of the encoding register and the contents of the decoding register on a stage-by-stage basis. If there is a lack of comparison, the modulo 2 adder at the input to the decoding register will yield a "1" in every stage of the decoding register which failed to match the contents of the encoding register. This, in turn, indicates that there is an error made in the reception of the complete message.

The minimum distance* of this particular code, as used for error detection, is seven. This means that it is guaranteed to detect

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6. W. W. Peterson, op. cit.

* The distance between two words is defined as the number of places in which they differ.

any error which involves the changing of six or fewer bits. If an error involves greater than six bits, the probability of satisfying the check bits may be considered to be 2^{-24} on the assumption that the bits are random when such an error occurs. The mean time to failure of the code may be determined by multiplying the probability of a word error containing more than six bits in error by 2^{-24}. Because of the bunching of errors, this probability is not simply related to the average bit error rate. This same code has an error-correcting distance of three but no effort is made in this system to utilize these properties.

Encoder and Decoder

A simplified block diagram of the combined ENCODER and word generator sections of the BC-1 is shown in Figure 5. The 1300-cps oscillator is shaped into pulses which are used for counting, shifting the feedback shift-register, and driving the receiver word generator through a gate which is open only during data time. The 224 bits comprising this section are derived by 14 consecutive scans of the 16 word-content switches, each one of which controls the state of one bit of the basic 16-bit sequence. For reasons to be discussed shortly, a "mark" is inserted into the data stream at "230" time, which is one of the service bit time-slots. During this time span from the 233rd through the 256th bit, the counter yields a signal which opens the feedback loop and gates the output of the encoding shift register to the DATA input of the dipulse modulator section where the interface signals are formed. The SYNC output is easily derived from the counter at "1" time.

Figure 6 is a simplified block diagram of the logical design of the DECODER and checkout sections. The SYNC, DATA, and TIMING dipulses are received by the DECODER from the demodulator and are immediately squared. After a delay equivalent to a 90° phase shift of the basic sinusoidal timing signal, the contents of the paralleled SYNC and DATA channels are sampled and the results stored in the associated flip-flop circuits. The data gate, which operates from the 6th through the 229th time slots, is now used to pass the received data to the comparison circuitry of the checkout section where they are

matched with the bits generated by the synchronized word generator. Mismatching will produce a "C" signal.

In the meantime, the incoming bits are forming the input to the decoding shift register; but due to practical circumstances, the decision to call a word in error cannot be based alone upon the results of scanning the decoding shift register. Two additional criteria must be used. The first concerns itself with the fact that the decoding of any "all-space" sequence will yield a "correct" decision upon the word. Since some data modems will yield such signals when there has been a dropout of the telephone circuit, such acceptance by the DECODER of these sequences must be guarded against. To solve this problem, a "mark" is inserted into the 230th position at the transmitter; the absence of a "mark" in that position at the receiver is sufficient reason for declaring that the entire word is in error, and the error is called a service bit error. The second additional criterion is based upon the fact that a word can only be accepted if proper synchronization has been maintained between the transmitter and receiver during the transmission of the word in question. The SYNC gate signals whether improper synchronization has occurred or if the synchronization is questionable. This is called SYNC error and it should be pointed out that poor design of, or complete disregard for, synchronization compromises the code to a considerable degree.

If all criteria have been satisfied, the word is declared "correct" at "1" time of the succeeding word. If the word is not correct, a "D" signal is emitted and comparison between the "C" and "D" signals is logically processed and the occurrence of the three principal combinations (CD, C'D and CD') are counted.

CD implies that both the bit-by-bit comparison and the decoding has agreed that the previous word has an error.

C'D indicates that the error which occurred was detected in the part of the word which is not subjected to the bit-by-bit comparison.

The CD' signal reveals that the decoding procedure failed to detect an error which was caught by bit-by-bit comparison.

The complete BC-1 is shown in Figure 7 with the encoding section in the upper portion of the rack and the decoding and checkout equipment in the lower portion.

Test Methods and Results

With the completion of the construction of the BC-1 system, circuit and system procedures were initiated since the use of the error-detection technique now places considerable importance on the reliability of terminal equipment. The usual line-filtering and shielding precautions were observed, in addition to reliable circuit design techniques. The impedance level on all transfer lines is no higher than 100 ohms. These precautions came naturally since the equipment is normally tested in a laboratory containing a teletype machine that is a prolific contributer of impulse noise and contiguous to a machine shop with heavy machine tools. Adequate ventilating of all circuits aboard was provided, with particular care given to power supply units. Maintenance of all mechanical parts can be performed without turning the unit off.

Since the nature of occurrence of errors on telephone lines is such that one might have to wait quite some time for a word error to appear, the debugging of the system was accelerated by using the back-to-back method indicated in Figure 8. By adjusting the noise generator such that the equivalent "on-line" signal-noise ratio was approximately 3 db, some of the logical faults of the decoder were quickly found. Most of these were the results of assuming the demodulator would deliver a sinusoidal signal with very little distortion. This assumption was not valid under the 3-db S/N environment in the case of the Code Translation Data System (CTDS) modem which derives its timing signal from the data, and the BC-1 logic had to be changed to allow for considerable distortion of the TIMING signal.

One technique used for the "mouse-trapping" of BC-1 error sources was the use of two tape recorders. The first recorder was a loop recorder which gave the equivalent of a five-second delay line and this recorder was placed directly on the signal at the input to the modem receiver. The second recorder was triggered on by the CD' signal and turned itself off several seconds later; it recorded the delayed line signal from the loop recorder. When a CD' error occurred, the tape from the second recorder was played into the modem receiver again and again until the cause of the error was determined. Such a technique is

very powerful, considering the fact that equipment of the BC-1 type when it is almost completely debugged will make only one error within a day or two. The error-detection technique also enables the designer to know when a catastrophic failure has occurred on a circuit board. Catastrophic failures in any of about 80 per cent of the circuit boards will cause the BC-1 to yield an ERROR signal at its output.

One more subtle error uncovered by the sensitivity of the code came from observing one or more errors occurring in groups at intervals of two to five weeks. These were ultimately traced to a faulty circuit that was intolerant of sudden line-voltage drops. This circuit has been tested prior to use, but the test method was disclosed as faulty by this operation.

Because of the power of the 3-db S/N test previously described for debugging, this same method was used as an accelerated equivalent of an "on-line" test. This test was conducted continuously for 571 hours, during which time 3,047,388 words were correctly detected as being in error. There was not a single undetected erroneous word. Using long-term average calculations based upon the characteristics of toll-grade telephone circuits, approximately sixty years of continuous transmission would be necessary to accumulate the total words in error that were correctly detected by the BC-1.

The next test was to check the high-level random noise capabilities of the unit. It consisted of 310 hours of continuous operation of the decoder when the model receiver had an input of high-level random noise. During the test period, 5,647,104 erroneous words were successfully detected without a single word in error being accepted as genuine.

When it was felt that adequate measures had been taken for guarding against equipment and logical malfunctions, the units were operated continuously for one week back-to-back with no intermediate modem without any errors. Then the modem was inserted, but with merely a jumper between the transmitter and receiver. This test lasted for another week. No errors of any sort were recorded in this two-week period.

The BC-1 has now been operating a total of 1515 hours on toll-grade telephone circuits in the New England area and, in this time, has correctly detected 6,707 words as being in error; there have been no undetected erroneous words.

Conclusion

Test results indicate that the codes may be successfully implemented in an on-line machine providing adequate care is taken to avoid compromising the code by false synchronization and, in addition, by a fail-safe approach to logical design. Extremely reliable circuitry is essential. The time devoted to the debugging program was considered shortened by use of the 3-db S/N method combined with varied "mouse-trapping" techniques; such approaches are suggested to all who are faced with similar systems problems.

Acknowledgment

The author is indebted to H. Sherman and R. G. Ticknap for their helpful discussions. Particular acknowledgment must be made to B. Reiffen and H. Yudkin upon whose work much of the BC-1 development is based. The extremely short time between paper design and the debugged unit is a tribute to the fine technical support given this effort by C. Breen, D. Chace and W. Lawler, who contributed most significantly in this regard. All are members of Group 25, Communications, of M.I.T. Lincoln Laboratory.

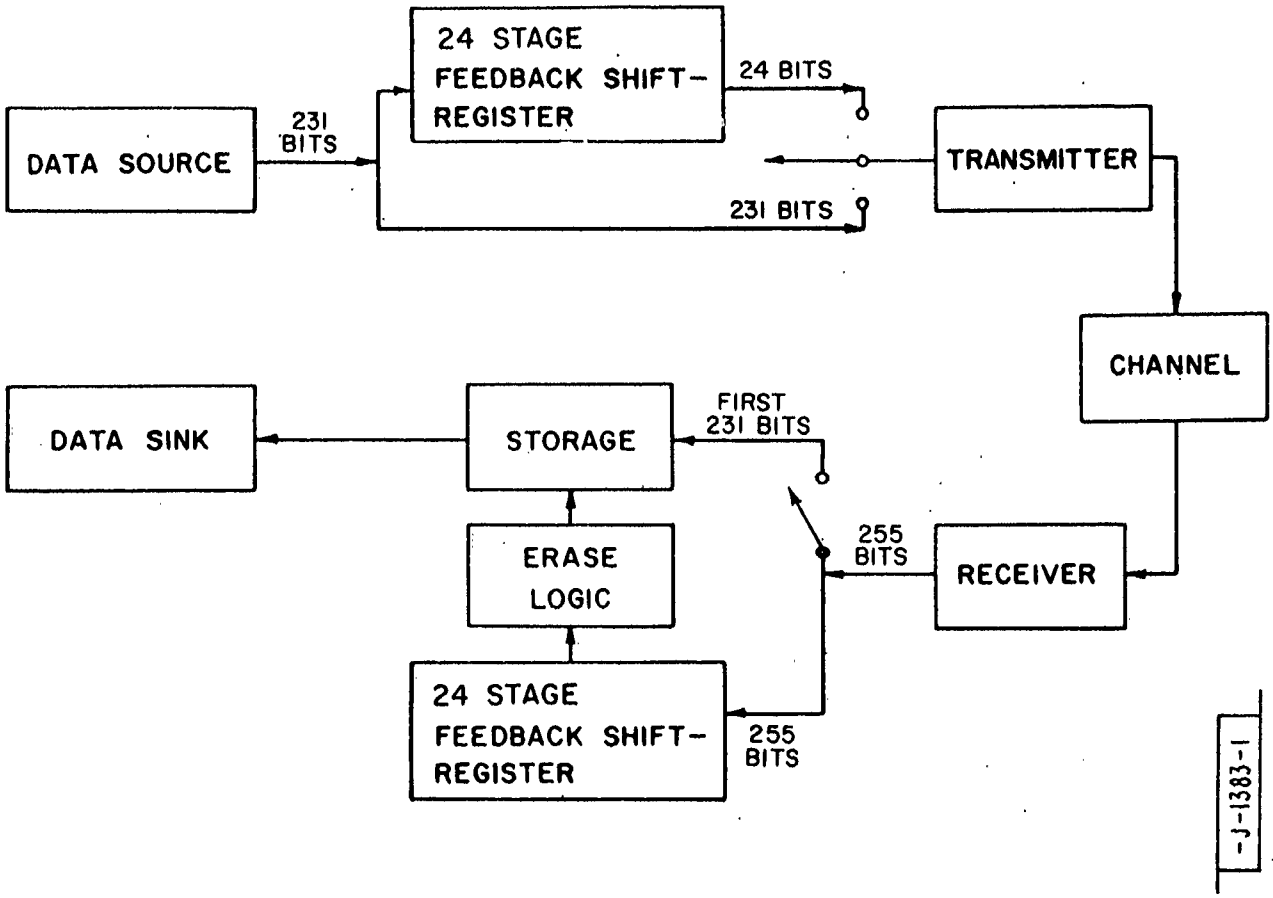

Fig. 1 General Bose-Chaudhuri Encoding and Decoding System

The data source provides an output of 231 bits. During this time the switch at the input of the modulator is in the lower position with the result that these bits are immediately operated upon by the modulator. Simultaneously, these bits form the input to the 24-stage encoder which is actually a shift register with linear feedback connections. At the end of the 231st bit, the data source stops and the switch reverts to its upper position, the feedback loops of the encoder are opened, and the 24 bits contained in the shift-register are shifted into the modulator.

The process at the demodulator is similar. During the first 231 bits, the switch at the output of the demodulator is closed, thereby allowing all the data bits to enter the word storage unit. The input to the DECODER consists of all 255 bits. The decoding shift register is identical to the feedback shift register that did the encoding and the feedback loop opens at the end of the 231st bit. At the end of the 255th bit, the error-detection logic scans the contents of the shift register and if a "mark" exists in any of the stages, then an error has taken place in the transmission. The ERROR signal is given to the data sink which is given the option of using the word in storage, knowing this word is most probably in error or, more simply, using the ERROR signal to erase the word in storage.

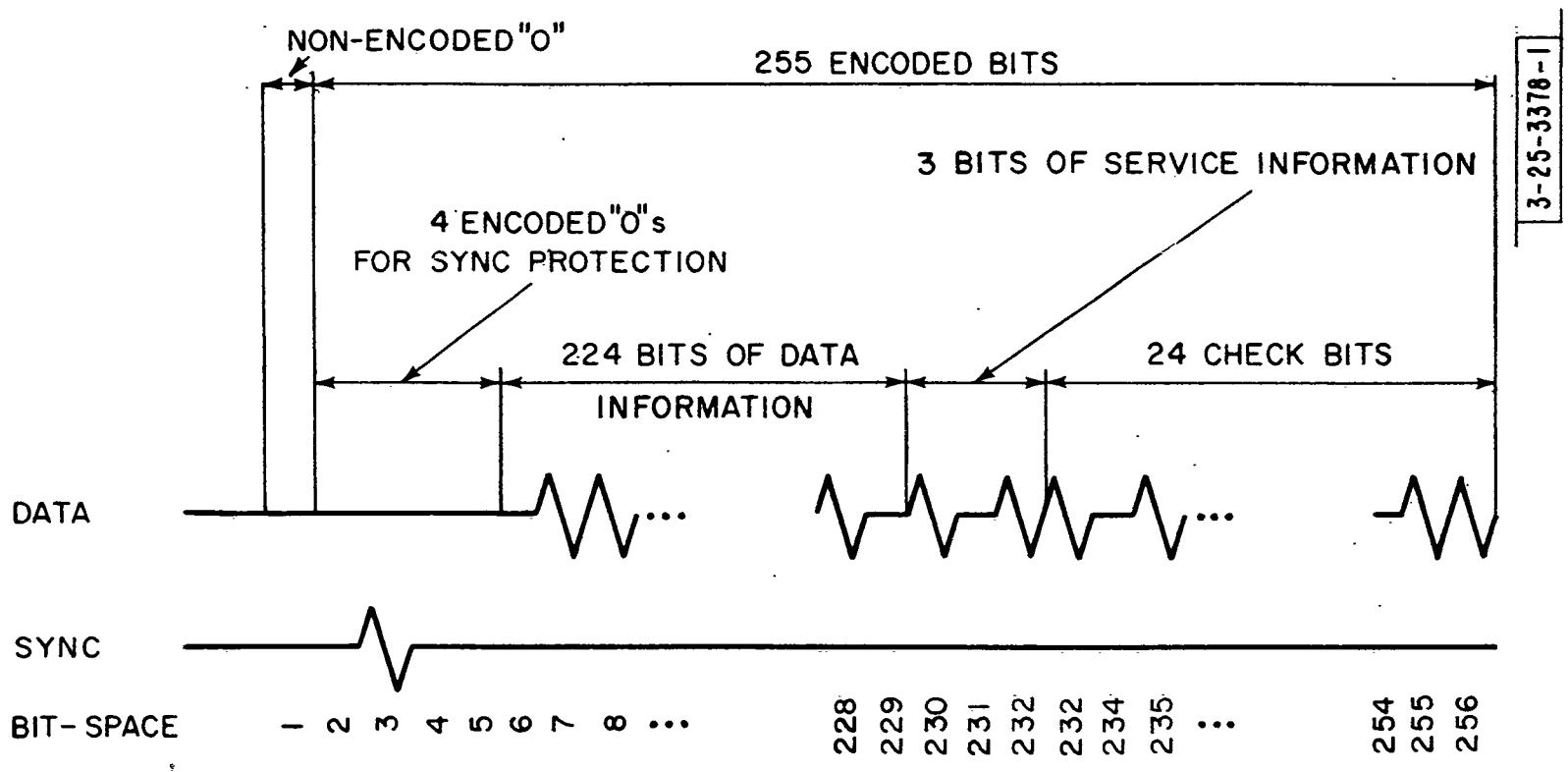

Fig. 2 Word Format

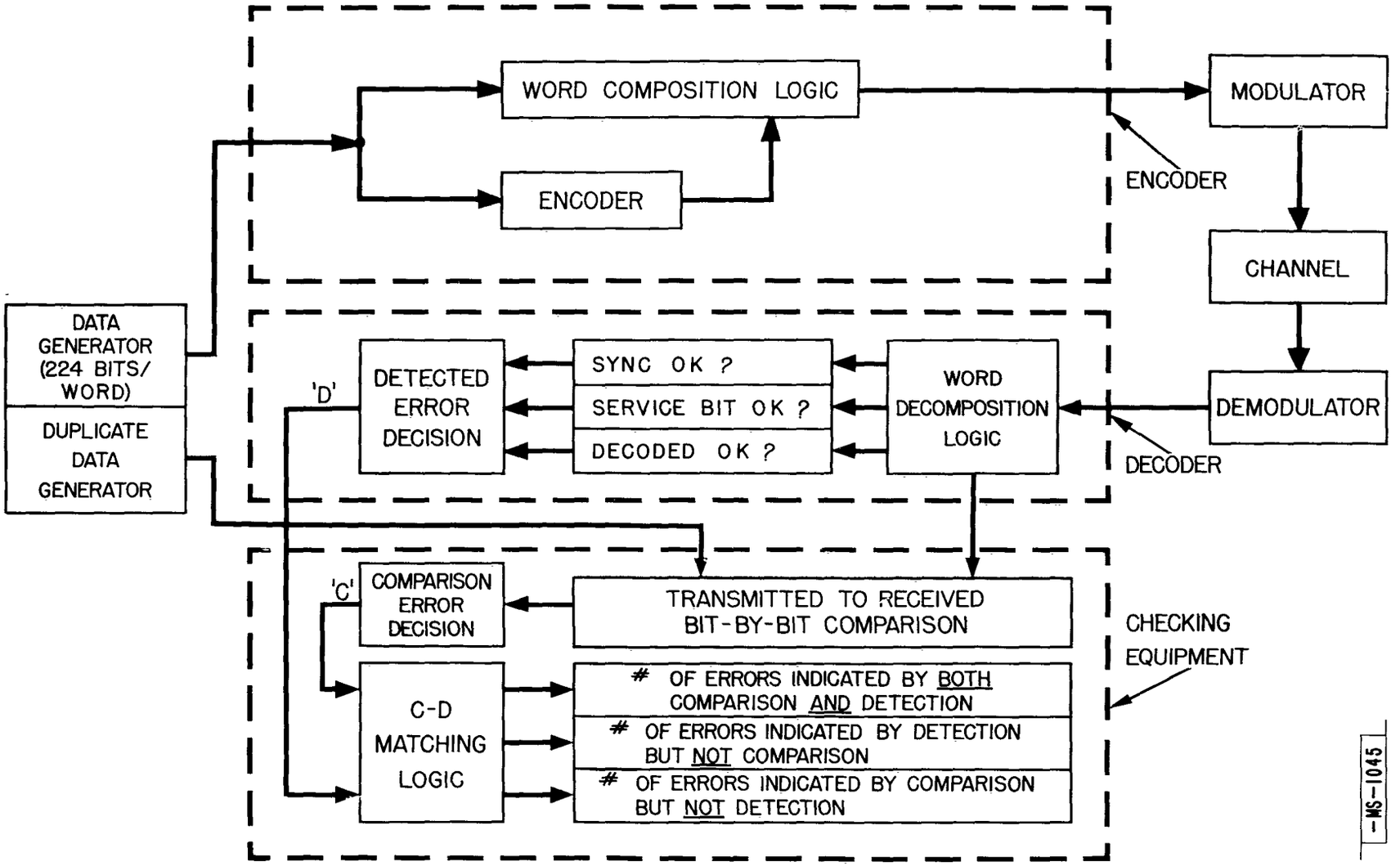

Fig. 3 Complete BC-1 System

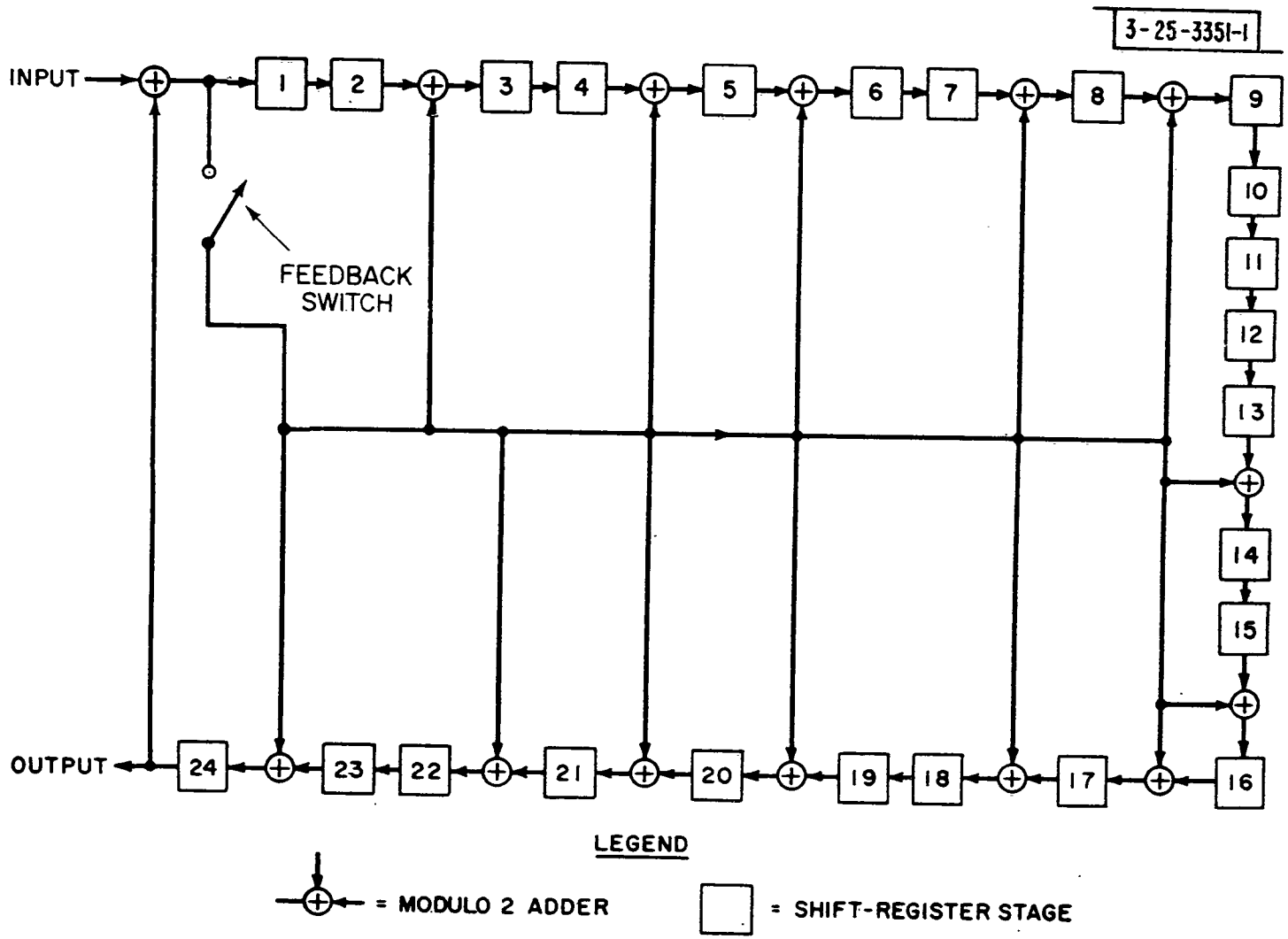

Fig. 4 Linear Feedback Shift-Register

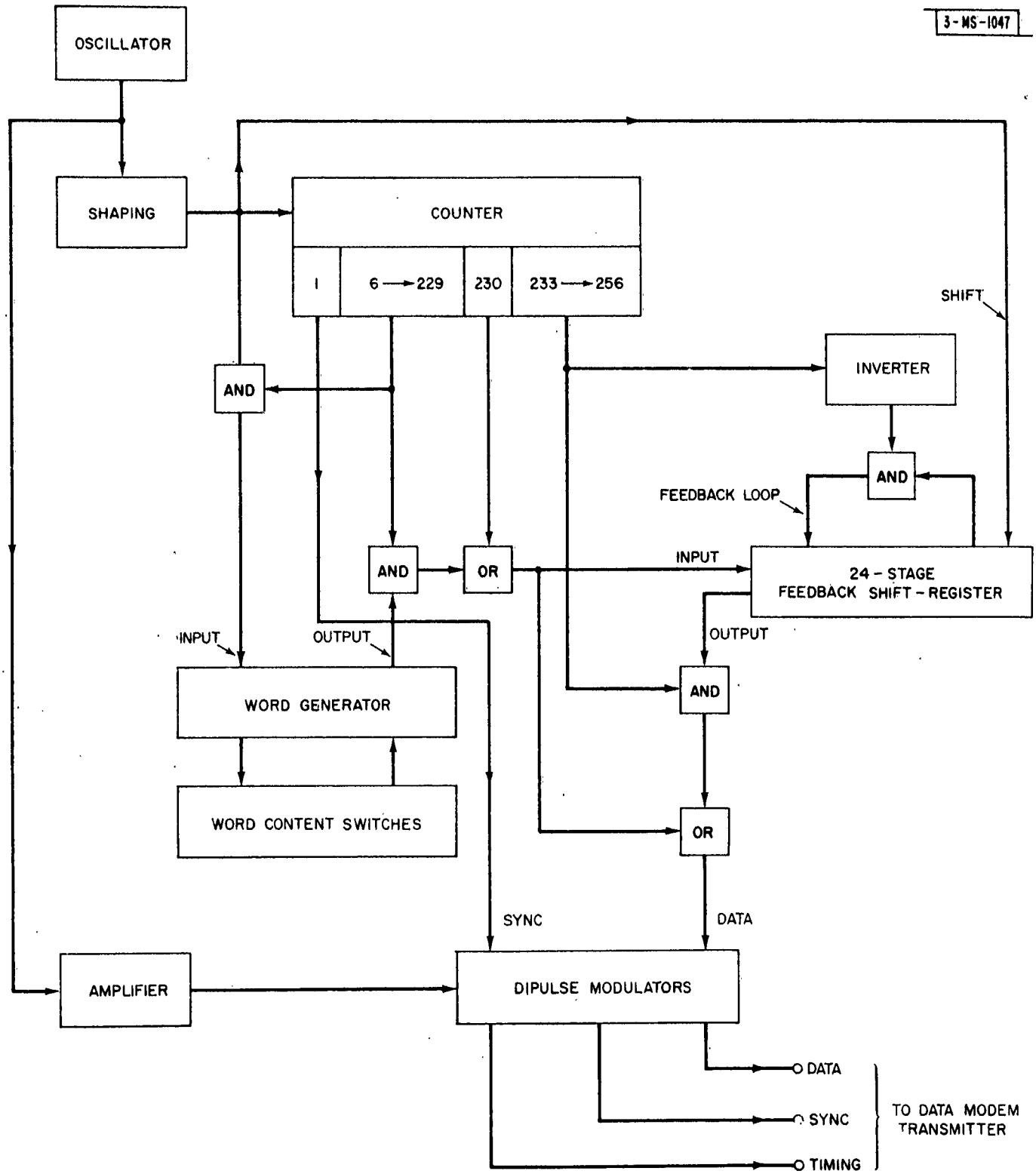

Fig. 5 ENCODER Block Diagram

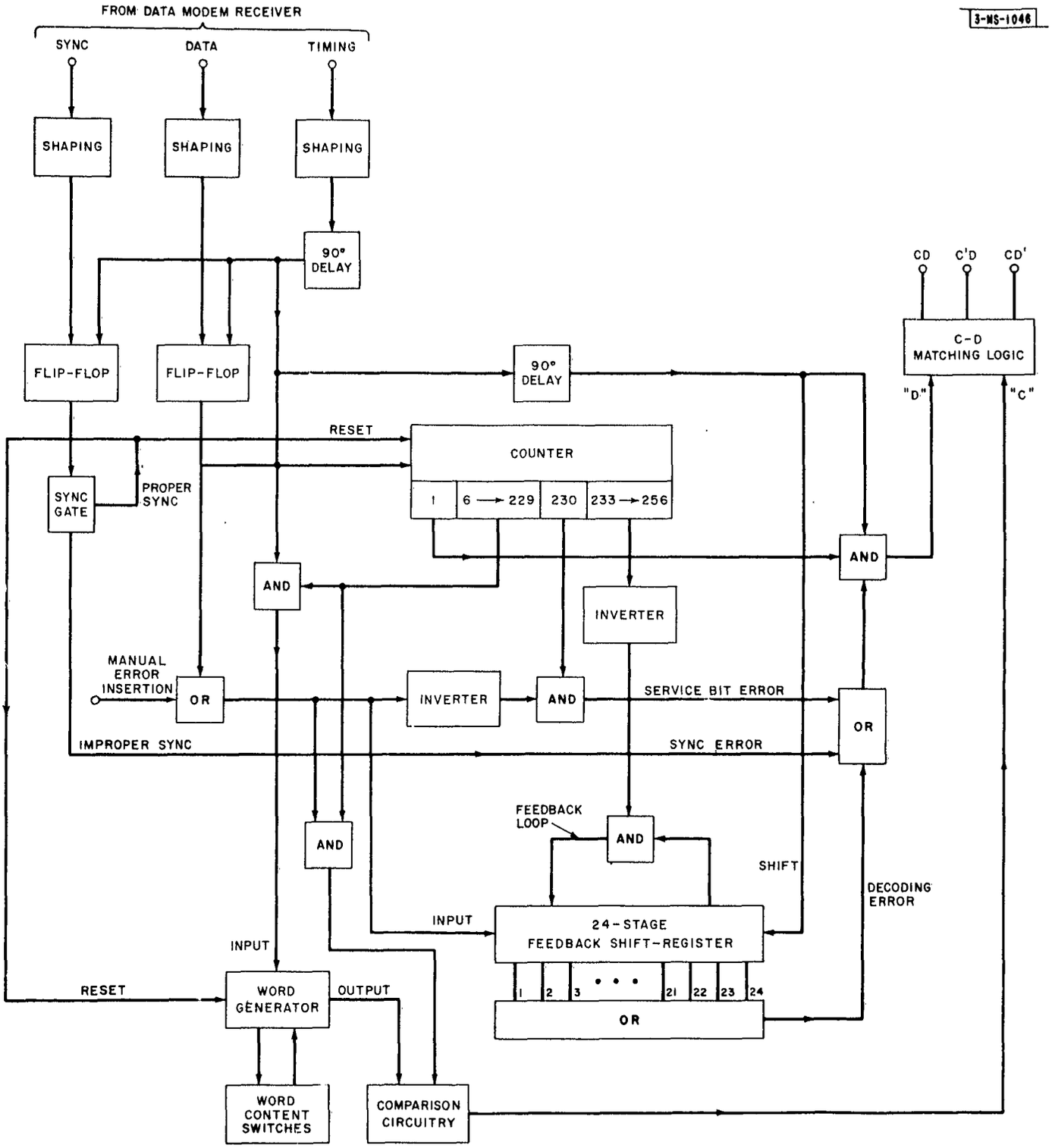

Fig. 6 DECODER Block Diagram

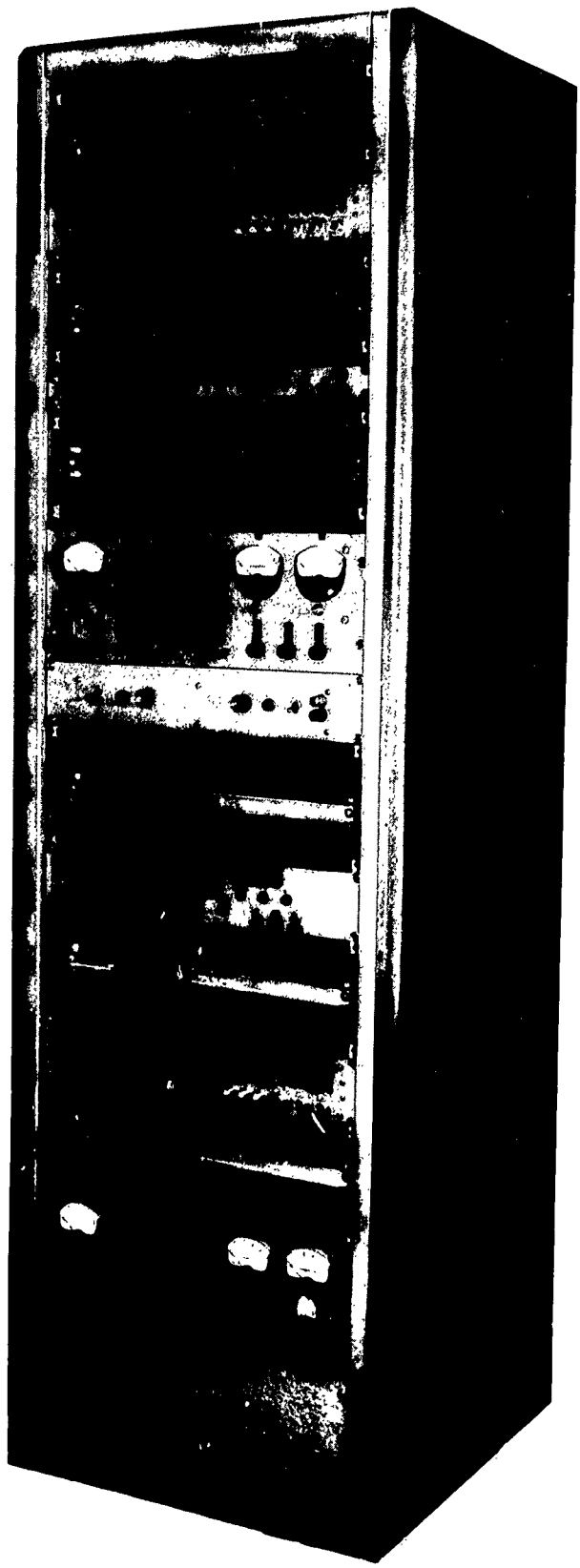

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Fig. 7 BC-1 Machine

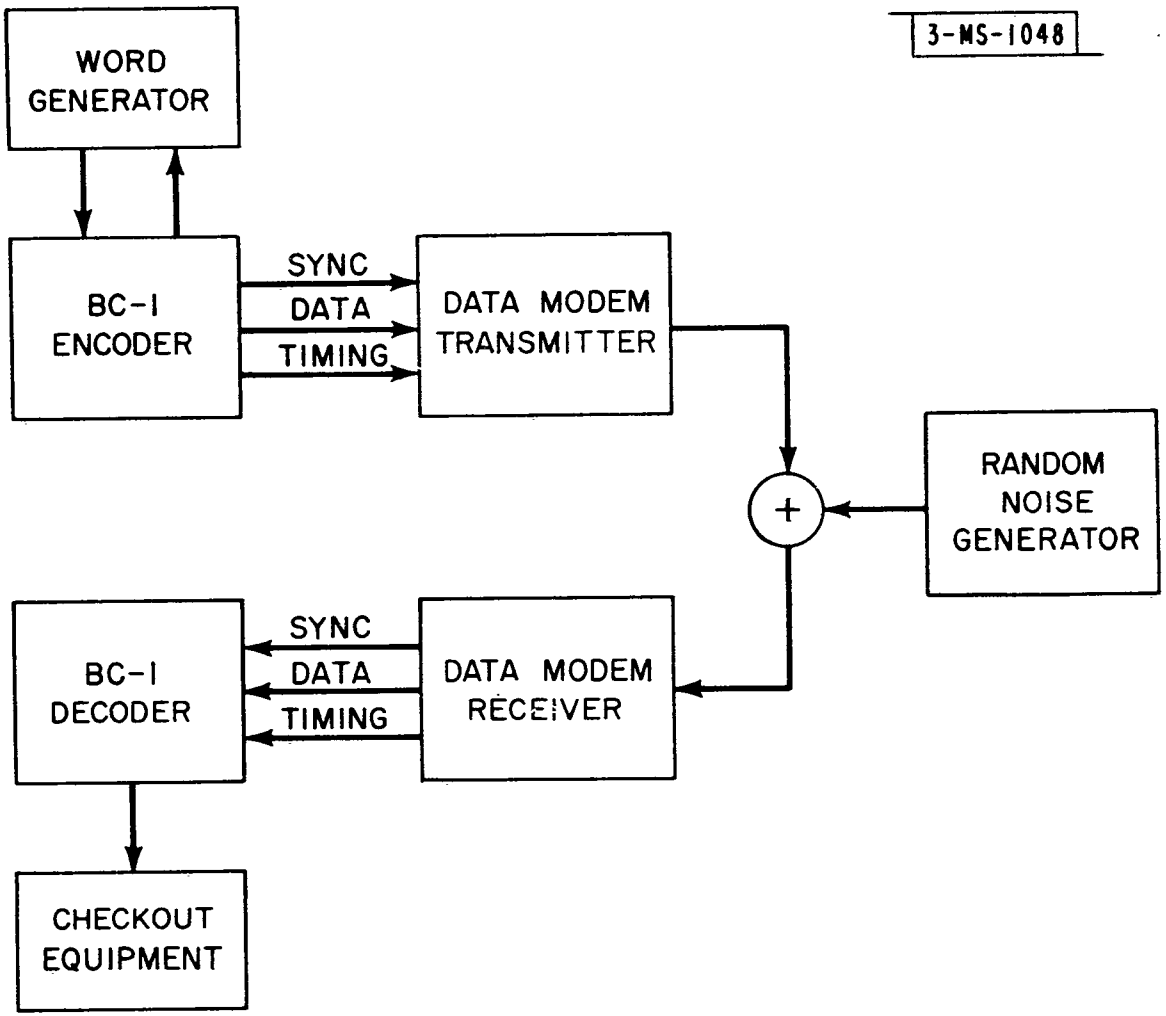

Fig. 8 Back-to-Back Debugging System

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